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EXAMINER	
CURS, NATHAN M	

ART UNIT	PAPER NUMBER
2633	12

DATE MAILED: 08/25/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/621,009	YANG ET AL.	
	Examiner	Art Unit	
	Nathan Curs	2633	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 July 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-8,11-13,15-17,19-32 and 34-40* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8,11-13,15-17,19-32 and 34-40* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *20 July 2000* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *3, 4 and 5*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claim 25 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Regarding claim 25, the phrase "outputting a delayed primary signal comprising the first signal, and the outputted primary signal comprising the second signal" is confusing.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 17, 19-24, 27-32, 36 and 37 are rejected under 35 U.S.C. 103(a) as being unpatentable over by Mokhtari et al. ("Bit-rate transparent electronic data regeneration in repeaters for high speed lightwave communication systems", Circuits and Systems, 1999. ISCAS '99. Proceedings of the 1999 IEEE International Symposium on, Volume 2, 30 May-2 June 1999, pages 508-511 vol. 2).

Regarding claim 17, Mokhtari et al. disclose a method of operating a receiver which functions independently of a bit rate of a received signal, comprising: receiving an original signal

(fig. 2, Data IN signal); generating a resultant signal by performing an exclusive-OR operation on a first signal and a second signal, said first signal corresponding to said original signal delayed by a predetermined quantity of time, said second signal corresponding to said original signal not delayed (fig. 5 and page 509, col. 2, paragraph 1); determining a bit rate of said original signal by low-pass filtering said resultant signal, and determining a voltage level of the low-pass filtered resultant signal (fig. 6 and page 509, col. 2, paragraph 3); generating a reference clock signal separate from said original signal and in dependence upon said determined bit rate (fig. 3, element Clock Out and fig. 6, element VCO1-VCO3); and recovering an input clock signal and data from said original signal in dependence upon said reference clock signal (figs, 3 and 4, element Decision Circuit).

Regarding claim 19, Mokhtari et al. disclose receiving an original signal comprising an input optical signal (page 508, col. 1, paragraphs 3 and 4; and col. 2, paragraph 3), where this system includes a converter to convert an input optical signal to an original electrical signal (page 508, col. 2, paragraph 4); outputting two duplicate signals substantially equivalent to the electrical signal, the two duplicate signals comprising a primary signal and a secondary signal (fig. 5); and delaying the primary signal by the predetermined quantity of time (fig. 5 and page 509, col. 2, paragraph 1), and outputting a delayed primary signal comprising the first signal (fig. 5).

Regarding claim 20, Mokhtari et al. disclose a 3R regenerator with optoelectric conversion at the signal input (page 508, col. 2, paragraph 4), and disclose the first, and second signals (fig. 5), where these signals are inherently electrical for a 3R regenerator with optoelectric conversion.

Regarding claim 21 and 24, Mokhtari et al. disclose a method corresponding to receiving optical signals having a plurality of different bit rates (page 508, col. 1, paragraphs 3 and 4, and col. 2, paragraph 3).

Regarding claims 22 and 30, Mokhtari et al. disclose an original signal received corresponding to a plurality of original signals received (page 508, col. 1, paragraphs 3, 4, and 6), the recovering of the input clock signal and data from the original signal being performed for the plurality of original signals received (fig. 3 and page 509, col. 1, paragraphs 3 and 4), the plurality of original signals received having a respective plurality of different bit rates (page 508, col. 1, paragraphs 3, 4, and 6).

Regarding claim 23, Mokhtari et al. disclose recovering of the input clock signal and data from the original signal performed for a plurality of original signals received (fig. 2, fig. 3, page 509, col. 1, paragraphs 3, 4, and 5), the plurality of original signals received having a respective plurality of different bit rates (page 508, col. 1, paragraphs 3, 4 and 6).

Regarding claims 27, 29, and 36, Mokhtari et al. disclose that the clock generator and clock generation method comprise a plurality of oscillators generating clocking signals of different frequencies and selectively operating the oscillators to generate the reference clock signal in dependence upon the bit rate detected by the identification unit (fig. 6 and col. 2, paragraph 4).

Regarding claim 28, Mokhtari et al. disclose a 3R regenerator receiving an input optical signal (page 508, col. 2, paragraph 3), where this system includes a converter to convert an input optical signal to an original electrical signal (page 508, col. 2, paragraph 4); an identification unit for receiving an electrical signal (fig. 3, elements Edge Detector and PLL), where the edge detector and PLL comprise an identification unit, for generating a first signal comprising an electrical signal delayed by a predetermined quantity of time and for generating a

second signal comprising an electrical signal not delayed (fig. 5), for forming a third signal by performing an exclusive-OR logic operation upon the first and second signals (fig. 5), and for detecting a bit rate in dependence upon the third signal and a clock generator for generating a reference clock signal in dependence upon the detected bit rate (fig. 3, fig. 6 and page 509, col. 2, paragraphs 3 and 4); and a recovery unit for recovering an input clock signal and data from the input optical signal in dependence upon the reference clock signal (fig. 3 and page 509, col. 1, paragraph 3). Mokhtari et al. disclose that the identification unit comprises: a first unit for delaying the original electrical signal and for performing the exclusive-OR operation upon the first and second signals and for forming the third signal (fig. 5); and a second unit for filtering the third signal, and for detecting the bit rate in dependence upon a voltage level of the filtered third signal (fig. 6 and page 509, col. 2, paragraph 4). Mokhtari et al. disclose a Reshaping/Limiting stage between the O/E converter and the identification unit, thus the electrical signal output from the O/E converter is the original signal, which passes through the disclosed Reshaping/Limiting stage before entering the identification unit. However, it would have been obvious to one of ordinary skill in the art at the time of the invention that, given the reshaping function inherent to the decision circuit of the Retiming block of Mokhtari et al., the separate Reshaping/Limiting block as disclosed could be removed as being redundant depending on the degree of distortion of the incoming signal, since the Retiming block both reshapes and retimes. In the case where the Retiming block performs all reshaping and retiming functions, the original output signal from the O/E converter would go directing to the Retiming block.

Regarding claim 31, Mokhtari et al. disclose an apparatus, comprising: a fiber optic system including electrical 3R regeneration (page 508, col. 1, paragraph 3 and 4, and col. 2, paragraph 3); where this system includes an optoelectric converter to convert an input optical signal to an original electrical signal (page 508, col. 2, paragraph 4).

Regarding claim 32, Mokhtari et al. disclose an identification unit corresponding to a bit rate identification unit (fig. 3 and 5, and page 509, col. 2, paragraph 1).

Regarding claim 37, Mokhtari et al. disclose that the filtering corresponds to low-pass filtering (page 509, col. 2, paragraph 4).

5. Claims 1-8, 11-13 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mokhtari et al. ("Bit-rate transparent electronic data regeneration in repeaters for high speed lightwave communication systems", Circuits and Systems, 1999. ISCAS '99. Proceedings of the 1999 IEEE International Symposium on, Volume 2, 30 May-2 June 1999, pages 508-511 vol. 2) in view of Ishihara (US Patent No. 5557648).

Regarding claim 1, Mokhtari et al. disclose an apparatus, comprising: a fiber optic system including an electrical 3R function (page 508, col. 2, paragraph 3 and 4, and col. 2, paragraph 3); where this system includes a converter for converting an input optical signal to an original electrical signal (page 508, col. 2, paragraph 4); an identification unit for receiving an electrical signal (fig. 3, elements Edge Detector and PLL), where the edge detector and PLL comprise an identification unit, for generating a first signal comprising an electrical signal delayed by a predetermined quantity of time and for generating a second signal comprising an electrical signal not delayed (fig. 5), for comparing the first and second signals and for forming a third signal in dependence upon the comparing of the first and second signals (fig. 5), and for detecting a bit rate in dependence upon the third signal (page 508, col. 1, paragraph 4 and page 509, col. 2, paragraphs 3 and 4); a clock generator for generating a separate reference clock signal in dependence upon the detected bit rate (fig. 6, element VCO Bank) and a recovery unit for recovering data from the input optical signal in dependence upon the reference clock signal (fig. 3, element Decision Circuit and page 509, col. 1, paragraph 3); wherein said identification

unit further comprises: a first unit for delaying said electrical signal, for performing an exclusive-OR operation upon said first and second signals, and for forming said third signal in dependence upon said exclusive-OR operation performed upon said first and second signals (fig. 5). Mokhtari et al. disclose a second unit comprising: a filter for filtering the third signal, and bit rate deriving unit for deriving the bit rate in dependence upon information related to a voltage level and a predetermined bit rate (fig. 6; and page 509, col. 2, paragraph 4). Mokhtari et al. disclose the reference clock being branched to the decision circuit and to a clock output. However, it would have been obvious to one of ordinary skill in the art at the time of the invention to output the recovered clock from the decision circuit, along with the recovered data, which modification at most would require simple, well known, inverter logic and another output from the decision circuit, in order to eliminate the need to branch the reference clock to the decision circuit and it's own separate output. Mokhtari et al. disclose a Reshaping/Limiting stage between the O/E converter and the identification unit, thus the electrical signal output from the O/E converter is the original signal, which passes through the disclosed Reshaping/Limiting stage before entering the identification unit. However, it would have been obvious to one of ordinary skill in the art at the time of the invention that, given the reshaping function inherent to the decision circuit of the Retiming block of Mokhtari et al., the separate Reshaping/Limiting block as disclosed could be removed as being redundant depending on the degree of distortion of the incoming signal, since the Retiming block both reshapes and retimes. In the case where the Retiming block performs all reshaping and retiming functions, the original output signal from the O/E converter would go directing to the Retiming block. Mokhtari et al. also disclose that the filter and bit rate deriving circuits that follow the compare circuit (fig. 3) are part of a phase-locked loop, but do not disclose an analog-to-digital converter. Ishihara discloses a phase lock loop including a bit rate deriving circuit that has an analog-to-digital converter receiving a filtered

signal and converting the filtered signal from an analog signal to a digital signal (fig. 23 and col. 15, lines 38-59). It would have been obvious to an artisan at the time of the invention to include the analog-to-digital converter, as taught by Ishihara, after the filter in the phase locked loop of Mokhtari et al., to digitize the filter output, providing the advantage of quantizing the voltage level to specific value by converting to digital.

Regarding claim 2, Mokhtari et al. disclose an apparatus corresponding to an optical receiver receiving optical signals having a plurality of different bit rates (page 508, col. 1, paragraphs 3 and 4).

Regarding claim 3, Mokhtari et al. disclose that the bit rate of the input optical signal corresponds to a transmission rate (page 508, paragraphs 1, 3 and 4).

Regarding claim 4, Mokhtari et al. disclose an amplifier for amplifying the original electrical signal received from the converter (page 508, col. 2, paragraph 4 to page 509, col. 1, paragraph 1).

Regarding claim 5, Mokhtari et al. disclose that the amplifier outputs the amplified electrical signal to the identification unit (page 508, col. 2, paragraph 4 to page 509, col. 1, paragraph 1; and fig. 1, fig. 3 and fig. 5).

Regarding claim 6, Mokhtari et al. disclose an apparatus, comprising: a fiber optic system including electrical 3R regeneration (page 508, col. 1, paragraph 3 and 4, and col. 2, paragraph 3); where this system includes an optoelectric converter to convert an input optical signal to an original electrical signal (page 508, col. 2, paragraph 4).

Regarding claim 7, Mokhtari et al. disclose an identification unit corresponding to a bit rate identification unit (fig. 3 and 5, and page 509, col. 2, paragraph 1).

Regarding claim 8, Mokhtari et al. disclose that the comparing performed by the identification unit corresponds to the identification unit performing an exclusive-OR logic operation upon the first and second signals (fig. 5).

Regarding claim 11, Mokhtari et al. disclose that the filtering corresponds to low-pass filtering (page 509, col. 2, paragraph 4).

Regarding claim 12, Mokhtari et al. disclose a unit corresponding to a bit rate identification signal generator (fig. 3 and fig. 6 and page 509, col. 2, paragraph 4), where the filter output inherently corresponds to a bit rate identification signal.

Regarding claim 13, Mokhtari et al. disclose a unit corresponding to a bit rate deriving unit (fig. 6 and page 509, col. 2, paragraph 4), where the unit including the bank of oscillators inherently derives a bit rate by tuning the VCO to the bit rate, based on the output signal from the filter.

Regarding claim 16, Mokhtari et al. disclose that the clock generator and clock generation method comprise a plurality of oscillators for generating clocking signals of different frequencies, said oscillators being selectively operated to generate the reference clock signal in dependence upon the bit rate detected by the identification unit (fig. 6 and col. 2, paragraph 4).

6. Claims 15, 26 and 35 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mokhtari et al. in view of in view of Ishihara, as applied to claims *** above, and further in view of Uda et al. (European Patent Office Publication No. 0342010).

Regarding claims 15 and 35, Mokhtari et al. disclose two duplicate signals substantially equivalent to the original electrical signal, the two duplicate signals comprising a primary signal and a secondary signal (fig. 5); a delay unit for receiving the primary signal, for delaying the primary signal by the predetermined quantity of time, and for outputting the primary signal, the

delayed primary signal comprising the first signal and the secondary signal corresponding to the second signal (fig. 5); and an operator unit for performing the exclusive-OR logic operation upon the first and second signals (fig. 5 and page 509, col. 2, paragraph 1). Mokhtari et al. do not disclose a buffer unit for receiving the original electrical signal and for outputting two signals. Uda et al. disclose a digital signal regenerator, including a primary signal and a secondary signal, delaying the primary signal, and an exclusive-OR logic operation upon the first and second signals (page 3, lines 17-21). Uda et al. also disclose an input buffer amplifier amplifying the original electrical signal and outputting two duplicate signals (page 3, line 17). It would have been obvious to an artisan at the time of the invention to include a buffer unit, as taught by Uda et al., prior to splitting the signals for the compare circuit, in order to raise the two split signals to the optimal levels for sending the signals to the compare circuit.

Regarding claim 26, Mokhtari et al. disclose a method, as described above, comprising: receiving an optical signal original signal using an optoelectric converter, converting the optic signal to an electrical signal, forming two duplicate signals and delaying one of the signals by a predetermined quantity of time. Mokhtari et al. do not disclose that the two duplicate signals are output from a buffer. Uda et al. also disclose input buffer amplifier amplifying the original electrical signal and outputting two duplicate signals (page 3, line 17). It would have been obvious to an artisan at the time of the invention to include a buffer unit, as taught by Uda et al., prior to splitting the signals for the compare circuit, in order to raise the two split signals to the optimal levels for sending the signals to the compare circuit.

7. Claims 34, and 38 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mokhtari et al. ("Bit-rate transparent electronic data regeneration in repeaters for high speed lightwave communication systems", Circuits and Systems, 1999. ISCAS '99. Proceedings of the

1999 IEEE International Symposium on, Volume 2, 30 May-2 June 1999, pages 508-511 vol. 2) in view of Ishihara (US Patent No. 5557648).

Regarding claims 34 and 38, Mokhtari et al. disclose a second unit comprising: a filter for filtering the signal output from the compare circuit, and determiner determining the bit rate in dependence upon the signal received from the filter (fig. 6; and page 509, col. 2, paragraph 4). Mokhtari et al. also disclose that the filter and determining circuits that follow the compare circuit (fig. 3) are part of a phase-locked loop, but do not disclose an analog-to-digital converter. Ishihara discloses a phase lock loop including a determining circuit that has an analog-to-digital converter receiving a filtered signal and converting the filtered signal from an analog signal to a digital signal (fig. 23 and col. 15, lines 38-59). It would have been obvious to an artisan at the time of the invention to include the analog-to-digital converter, as taught by Ishihara, after the filter in the phase locked loop of Mokhtari et al., to digitize the filter output, providing the advantage of quantizing the voltage level to specific value by converting to digital.

8. Claims 39 and 40 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mokhtari et al. ("Bit-rate transparent electronic data regeneration in repeaters for high speed lightwave communication systems", Circuits and Systems, 1999. ISCAS '99. Proceedings of the 1999 IEEE International Symposium on, Volume 2, 30 May-2 June 1999, pages 508-511 vol. 2) in view of Ishihara (US Patent No. 5557648) as applied to claims 14, 34 and 38 above, and further in view of Uda et al. (European Patent Office Publication No. 0342010).

Regarding claim 39, Mokhtari et al. disclose two duplicate signals substantially equivalent to the original electrical signal, the two duplicate signals corresponding to a primary signal and a secondary signal (fig. 5); a delay unit receiving the primary signal, delaying the primary signal by the predetermined quantity of time, outputting the primary signal, the delayed

primary signal corresponding to the first signal (fig. 5); and an operator unit performing the exclusive-OR logic operation upon the first and second signals (fig. 5 and page 509, col. 2, paragraph 1). Mokhtari et al. do not disclose a buffer unit receiving the original electrical signal and outputting two signals. Uda et al. disclose a digital signal regenerator, including a primary signal and a secondary signal, delaying the primary signal, and an exclusive-OR logic operation upon the first and second signals (page 3, lines 17-21). Uda et al. also disclose input buffer amplifier amplifying the original electrical signal and outputting two duplicate signals (page 3, line 17). It would have been obvious to an artisan at the time of the invention to include a buffer unit, as taught by Uda et al., prior to splitting the signals for the compare circuit, in order to raise the two split signals to the optimal levels for sending the signals to the compare circuit.

Regarding claim 40, Mokhtari et al. disclose that the clock generator and clock generation method comprise a plurality of oscillators generating clocking signals of different frequencies and selectively operating the oscillators to generate the reference clock signal in dependence upon the bit rate detected by the identification unit (fig. 6 and col. 2, paragraph 4).

Response to Arguments

9. Applicant's arguments referred to below, filed 22 July 2004, have been fully considered but they are not persuasive.

Regarding the applicant's argument on page 23, lines 1-6 of the 22 July 2004 amendment, the applicant states "by way of further distinguishing the invention from the prior art cited by the Examiner, it is noted..."; however, the remainder of this paragraph only describes the Mokhtari et al. reference, not distinguishing the reference from the applicant's claimed invention, except by saying that "retime" or "retiming" as used by Mokhtari et al. has a different meaning from the meaning of "retiming" as disclosed in the present application. However this

argument is not convincing because the applicant doesn't distinguish the different meanings for "retiming".

Regarding the applicant's argument on page 23, lines 8-17 of the 22 July 2004 amendment, the applicant argues that the applicant's claimed invention is distinguished from Mokhtari et al. because an accurate reference clock is generated from a separate reference clock generator or separately. However, Mokhtari et al. does disclose a separate reference clock generator as claimed, specifically the selected VCO from the "bank" of VCOs used to produce the reference clock based on the detected bit rate (Mokhtari et al.: fig. 6 and page 509, col. 2, paragraph 3).

Regarding the applicant's arguments on page 34, lines 7-11 of the 22 July 2004 amendment, after mentioning the output of the LPF of the applicant's claimed invention being converted to a digital signal, the applicant argues that Mokhtari et al. do not disclose this limitation. However, as previously described, the combination of Mokhtari et al. in view of Ishihara et al. teach the output of the LPF converted to a digital signal. Arguments against references individually when an obviousness rejection is based on combination of references does not show non-obviousness. Further the applicant argues that Mokhtari et al. fail to disclose the use of the voltage level from the LPF and reorganization of the bit rate according to the voltage level. However, as shown in fig. 6a of Mokhtari et al, the output of the VCO from the "bank" of VCOs (used to produce the reference clock) is determined by the voltage level.

Applicant's further arguments with respect to claims 1, 17 and 28 (amendment of 22 July 2004: page 24, line 13 to page 26, line 12) have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

10. Any inquiry concerning this communication from the examiner should be directed to N. Curs whose telephone number is (703) 305-0370. The examiner can normally be reached on M-F (from 9 AM to 5 PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jason Chan, can be reached at (703) 305-4729. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-4700.

M. R. SEDIGHIAN
PRIMARY EXAMINER